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DATA SHEET

SAA4945H
LIne MEmory noise Reduction IC (LIMERIC)

Preliminary specification
File under Integrated Circuits, IC02

1997 Jun 10

Philips Semiconductors

PHILIPS

LIne MEmory noise Reduction IC (LIMERIC)

SAA4945H

FEATURES

- 2-D adaptive vertically recursive noise reduction
- Noise reduction for Y, U and V signals in 4 : 1 : 1 format
- Single 5 V ±10% power supply
- Communication by means of serial communication protocol 83C654 (SNERT bus)
- Via SNERT bus, 10 different types of noise reduction selectable; the noise reduction function can also be disabled
- Phase relation write enable input/output signal simultaneously switchable over one clock period w.r.t. input/output samples
- 8-bit wide data processing for Y, U and V; in unsigned format (Y signal) and in 2's complement (U and V signals)
- One fixed line locked clock operation frequency up to 16 MHz (typical)
- Exactly one line delay.

GENERAL DESCRIPTION

The SAA4945H, LIMERIC (LIne MEmory noise Reduction IC) is a 2-D recursive noise reduction filter for both luminance and colour difference signals. The noise reduction is automatically adapted to the global noise level in the image. Ten different preferences of noise reduction can be set using a synchronous receiver transmitter bus; SNERT (Synchronous No parity Eight bit Receive Transmit) bus. Alternatively, the noise reduction can be switched off. The LIMERIC is generally placed directly after the ADC in the feature box and works fully in the $1f_h$ (50/60 Hz) domain.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage (pins 5, 29 and 30)		4.5	5.0	5.5	V
I_{DD}	supply current		–	70	–	mA
P	power dissipation		–	350	–	mW
f_{CLK}	clock frequency	±7%; note 1	10	16	17.1	MHz
f_{SNERT}	bus clock frequency		–	–	1	MHz
T_{amb}	operating ambient temperature		0	–	70	°C

Note

1. Maximum number of clocks per line is 1024.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAA4945H	QFP44	plastic quad flat package; 44 leads (lead length 1.3 mm); body 10 × 10 × 1.75 mm	SOT307-2

BLOCK DIAGRAM

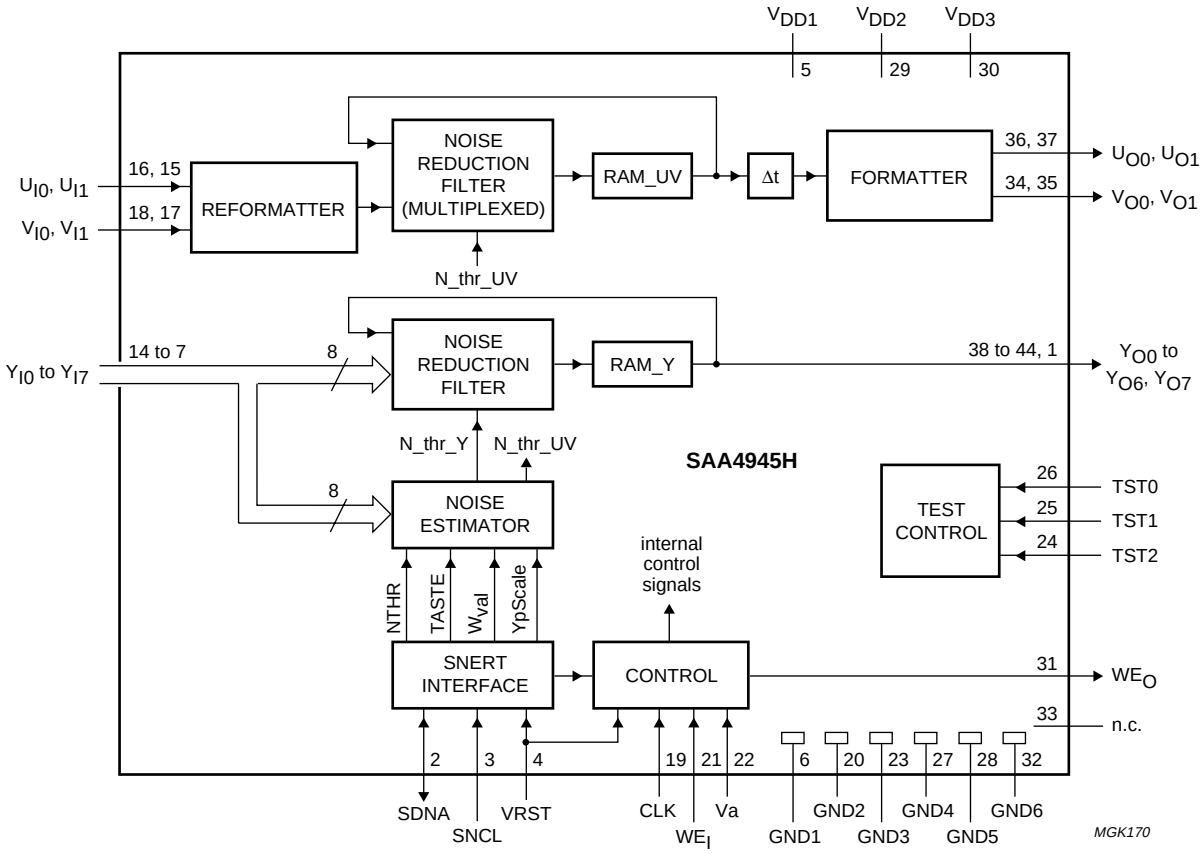


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	TYPE	DESCRIPTION
Y_{O7}	1	output	luminance output bit 7
SNDA	2	input/output	data from interface SNERT bus
SNCL	3	input	clock from interface SNERT bus
VRST	4	input	reset in the vertical blanking interval
V_{DD1}	5	supply	supply voltage 1
GND1	6	ground	ground 1
Y_{I7}	7	input	luminance input bit 7 from analog-to-digital converter
Y_{I6}	8	input	luminance input bit 6 from analog-to-digital converter
Y_{I5}	9	input	luminance input bit 5 from analog-to-digital converter
Y_{I4}	10	input	luminance input bit 4 from analog-to-digital converter
Y_{I3}	11	input	luminance input bit 3 from analog-to-digital converter
Y_{I2}	12	input	luminance input bit 2 from analog-to-digital converter
Y_{I1}	13	input	luminance input bit 1 from analog-to-digital converter
Y_{I0}	14	input	luminance input bit 0 from analog-to-digital converter
U_{I1}	15	input	U input bit 1 from analog-to-digital converter
U_{I0}	16	input	U input bit 0 from analog-to-digital converter
V_{I1}	17	input	V input bit 1 from analog-to-digital converter
V_{I0}	18	input	V input bit 0 from analog-to-digital converter
CLK	19	input	master clock
GND2	20	ground	ground 2
WE_I	21	input	write enable input
Va	22	input	vertical blanking pulse
GND3	23	ground	ground 3
TST2	24	input	test pin 2
TST1	25	input	test pin 1
TST0	26	input	test pin 0
GND4	27	ground	ground 4
GND5	28	ground	ground 5
V_{DD2}	29	supply	supply voltage 2
V_{DD3}	30	supply	supply voltage 3
WE_O	31	output	write enable output
GND6	32	ground	ground 6
n.c.	33	–	not connected
V_{O0}	34	output	V output bit 0
V_{O1}	35	output	V output bit 1
U_{O0}	36	output	U output bit 0
U_{O1}	37	output	U output bit 1
Y_{O0}	38	output	luminance output bit 0
Y_{O1}	39	output	luminance output bit 1
Y_{O2}	40	output	luminance output bit 2

SYMBOL	PIN	TYPE	DESCRIPTION
Y_{O3}	41	output	luminance output bit 3
Y_{O4}	42	output	luminance output bit 4
Y_{O5}	43	output	luminance output bit 5
Y_{O6}	44	output	luminance output bit 6

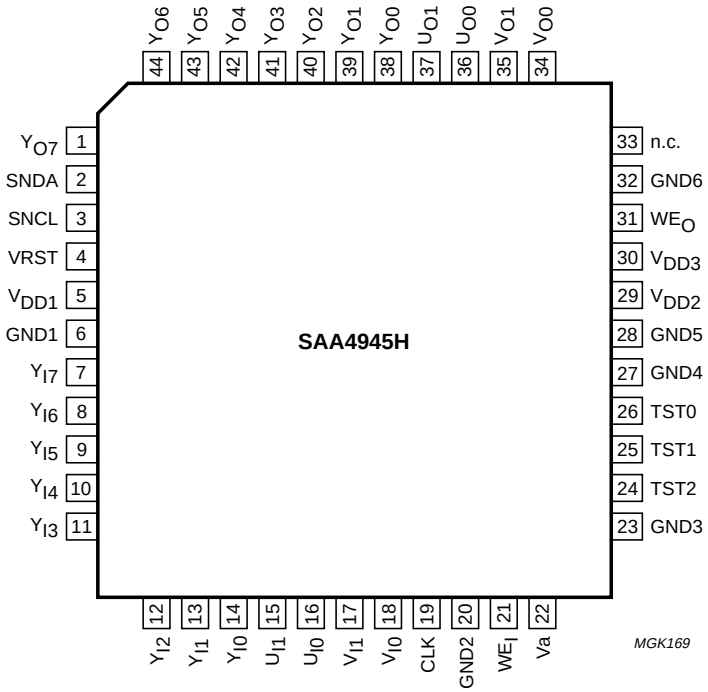


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The digital LIMERIC is an effective low noise reduction IC for luminance and colour difference signals. Noise filtering is automatically adapted to the global noise level which is measured within the picture content. The two dimensional non-linear noise reduction (one for luminance, one for chrominance) uses only line memory to function. Furthermore, up to 10 different preferences can be set by the user.

As shown in Fig.1, the main components of the device are the noise reduction filter with the line memories (RAM) and the noise estimator. Other components shown are the reformatter, formatter, controller and a SNERT bus transceiver.

Noise reduction filter

Both luminance and chrominance signals are filtered with **vertical recursion**. This is produced as the filter receives both filtered samples from the previous line, and unfiltered samples from the current line. A new replacement value is calculated for each sample read from the **line memory**. This in turn, is the filtered response value for the reference input pixel. The reference pixel is then placed at the centre of the delay-line into which the current (unfiltered) video line is shifted. Tables 1 to 6 show this as an 'O'.

Both luminance and colour difference signals are filtered using the so-called **D**iscriminating **A**veraging **F**ilter (DAF), in which filter coefficients are related to the **A**bsolute **D**ifference (AD) between samples. The filter uses samples from both present and previous line (using the line delay) and the result of the filter is stored back in the line memory. In this way a vertical recursive structure is realized.

The filter coefficients are set depending on the noise measured by the noise estimator or the NTHR (SNERT register F9).

CHROMINANCE FILTER

The basic signal processing for either U or V is via the same filter. It is used to process both V and U using a multiplexed operation.

The taps structure of the chrominance filter is as shown in Table 1.

Table 1 Chrominance processing

X X X X X	← 5 adjacent R – Y samples from the filtered line
o O o	← 3 adjacent R – Y samples from the incoming line

LUMINANCE FILTER

The taps structure of the luminance filter is as shown in Table 2.

Table 2 Luminance processing

X . . . . X . . . X . . . X X	← 5 Y samples from the filtered line (distance 4 / 5 pixel)
o . O . o	← 3 Y samples from the incoming line (distance 2 pixels)

A 'weave' function is used to reduce any smearing effect that could occur at edges. As shown in Tables 3 to 6, the 'weave' calculates over 4 consecutive lines. The relative position of the actual pixel changes one position every line.

Table 3 For line 2n

X . . . . X . . . X . . . X X
o . O . o

Table 4 For line 2n + 1

X . . . . X . . . X . . . X X
. . o . O . o

Table 5 For line 2n + 2

X . . . . X . . . X . . . X X
o . O . o

Table 6 For line 2n + 3

X . . . . X . . . X . . . X X
o . O . o . .

Table 7 Weave configuration

Depending on even and odd fields the 'weave' has the following configuration:

ODD FIELDS	EVEN FIELDS
X	X
X	X
X	X
X	X
X	X
X	X
X	X

Noise estimator

The threshold value N_thr for the filters is calculated in the noise estimator block (see Fig.3). There are four options for producing the N_thr value:

1. Pre-filter gain setting (YpScale)
2. W_{val} selects the sensitivity of the noise estimator
3. TASTE (TS) scales the N_thr linear
4. NTHR is externally applied when the noise estimator is disabled by the control bit ExThr of the Status Register.

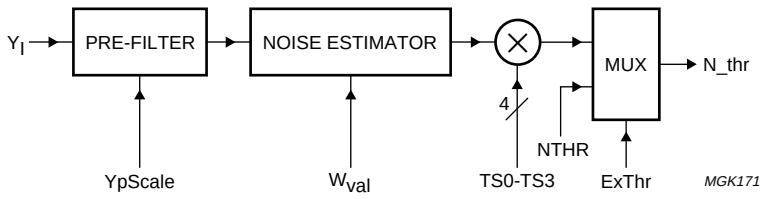


Fig.3 Noise estimator.

SIGNAL DESCRIPTION

Input signals

Y_{I7} TO Y_{I0} (PINS 7 TO 14)

- Eight bit wide digital luminance input bus
- Unsigned data; dynamic range between 0 and 255
- The maximum number of input samples equals 852 active samples/line.

U_{I1} AND U_{I0} (PINS 15 AND 16)

- Colour difference signal U
- Data in 2's complement; dynamic range between –128 and +127
- Y : U : V format 4 : 1 : 1; see Table 8 for input data coding
- The maximum number of input samples equals 213 samples/line
- Internal data processing of U signals in unsigned format.

V_{I1} AND V_{I0} (PINS 17 AND 18)

- Colour difference signal V
- Data in 2's complement; dynamic range between –128 and +127
- Y : U : V format 4 : 1 : 1; see Table 8 for input data coding
- The maximum number of input samples equals 213 samples/line
- Internal data processing of V signals in unsigned format.

Table 8 Input /output data coding

INPUT	BIT	INPUT DATA SEQUENCE			
Y	Y7	$Y_0$7	$Y_1$7	$Y_2$7	$Y_3$7
	Y6	$Y_0$6	$Y_1$6	$Y_2$6	$Y_3$6
	Y5	$Y_0$5	$Y_1$5	$Y_2$5	$Y_3$5
	Y4	$Y_0$4	$Y_1$4	$Y_2$4	$Y_3$4
	Y3	$Y_0$3	$Y_1$3	$Y_2$3	$Y_3$3
	Y2	$Y_0$2	$Y_1$2	$Y_2$2	$Y_3$2
	Y1	$Y_0$1	$Y_1$1	$Y_2$1	$Y_3$1
	Y0	$Y_0$0	$Y_1$0	$Y_2$0	$Y_3$0
U	UI1	$U_0$7	$U_0$5	$U_0$3	$U_0$1
	UI0	$U_0$6	$U_0$4	$U_0$2	$U_0$0
V	VI1	$V_0$7	$V_0$5	$V_0$3	$V_0$1
	VI0	$V_0$6	$V_0$4	$V_0$2	$V_0$0

WE_I (PIN 21)

- Write enable input
- Write enable indicates the time when active input samples (Y, U and V) are present
- Timing relation (see Fig.4) depending on the logic level of the **W**rite **E**nable **S**elect signal (WES) in status register; to adapt to different external video memories
- The number of input samples is a multiple of 4 (see Fig.4)
- Start of new line indicated by write enable signal LOW for at least 4 consecutive clock periods (see Fig.4)
- During active line, WE_I is not allowed to be LOW for more than 1 clock cycle.

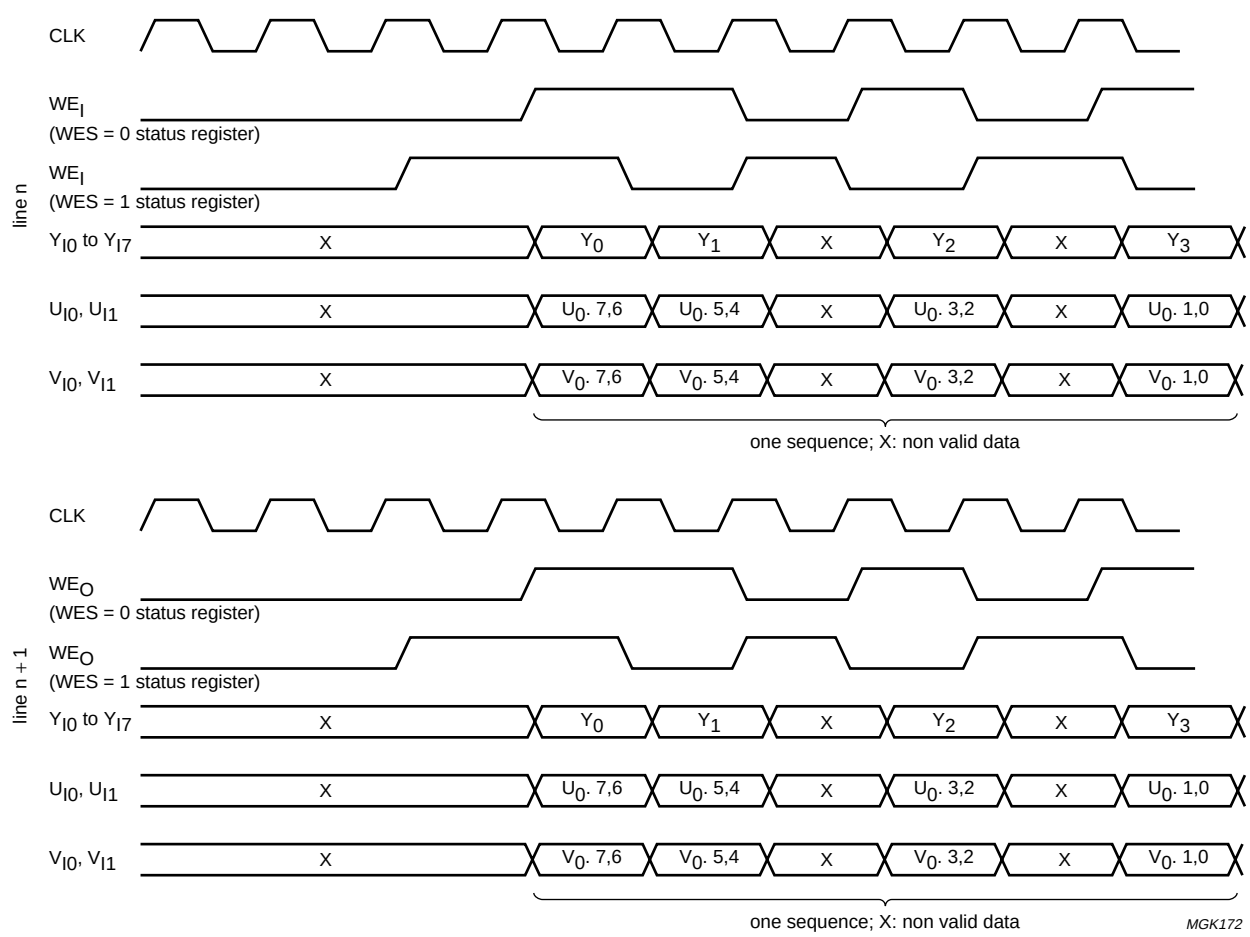


Fig.4 Write enable timing.

Va (PIN 22)

- Vertical synchronization signal, active HIGH
- Minimum HIGH period equals one line period
- Vertical synchronization signals converted to system clock domain internally. So the Va pulse can be asynchronous.
- See timing diagram Fig.6 and Table 11 for timing specification.

CLK (PIN 19)

- Line locked system clock, up to 16 MHz typical
- All clock related signals act on the rising edge of the system clock.

TST0, TST1 AND TST2 (PINS 26, 25 AND 24)

- Test mode inputs
- Active HIGH, with internal pull-down resistors.

Table 9 Test settings

TST2	TST1	TST0	MODE
0	0	0	application mode
X(1)	1	X(1)	test mode
1	X(1)	X(1)	test mode
X(1)	X(1)	1	test mode

Note

1. X = don't care.

SNDA, SNCL AND VRST (PINS 2, 3 AND 4)

- Serial interface signals
- SNERT bus protocol (Synchronous No parity 8-bit receiver and Transmission bus)
- SNDA is a bidirectional signal with 8-bit wide data and address (LSB first)
- Serial interface signals converted (internally) to system clock domain. To avoid set-up violations these signals are clocked two times by the system clock before further processing is performed.
- Synchronization of serial address (every even byte) and data (every odd byte) by VRST.

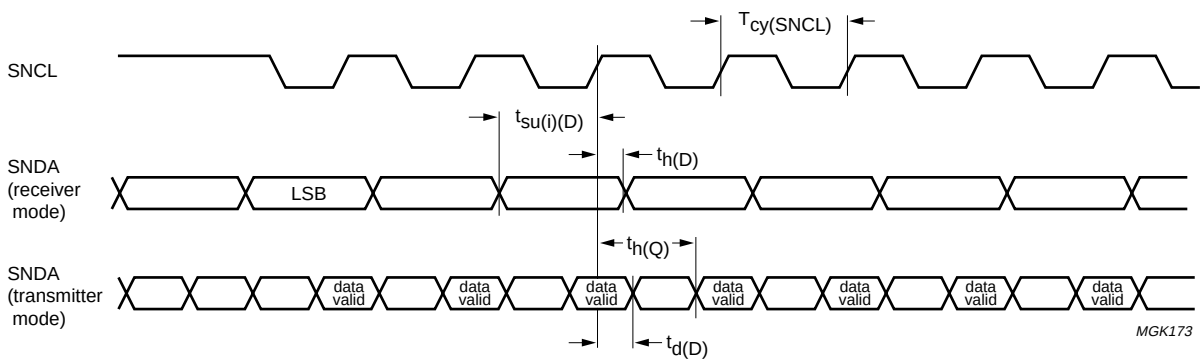


Fig.5 Timing diagram of serial interface.

Table 10 Timing characteristics (see Fig.5)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
$t_{cy(SNCL)}$	SNCL cycle time	1	–	µs
$t_{su(i)(D)}$	input set-up time	90	–	ns
$t_{h(D)}$	input hold time	50	–	ns
$t_{h(Q)}$	output data hold time	0	–	ns
$t_{d(D)}$	output data delay time	–	700	ns

Output signals

Y_{O0} TO Y_{O7} (PINS 38 TO 44 AND 1)

- 8-bit wide digital luminance output bus
- Data format: unsigned, dynamic range between 0 and 255.

U_{O1} AND U_{O0} (PINS 37 AND 36)

- Colour difference signal U
- Data format: 2's complement, dynamic range between –128 and +127
- Y : U : V format 4 : 1 : 1; see Table 8.

V_{O1} AND V_{O0} (PINS 35 AND 34)

- Colour difference signal V
- Data format: 2's complement, dynamic range between –128 and +127
- Y : U : V format 4 : 1 : 1; see Table 8.

WE_O (PIN 31)

- Write enable output
- Write enable indicates the time when active samples (Y, U and V) are present
- Timing relation (see Fig.6) depending on write enable select signal (WES) in status register; to adapt to different external video memories
- The number of output samples is a multiple of 4
- The write enable output sequence is a copy of the write enable input sequence of the previous line (see Fig.6) with a shift of one line
- The last line in field is not processed.

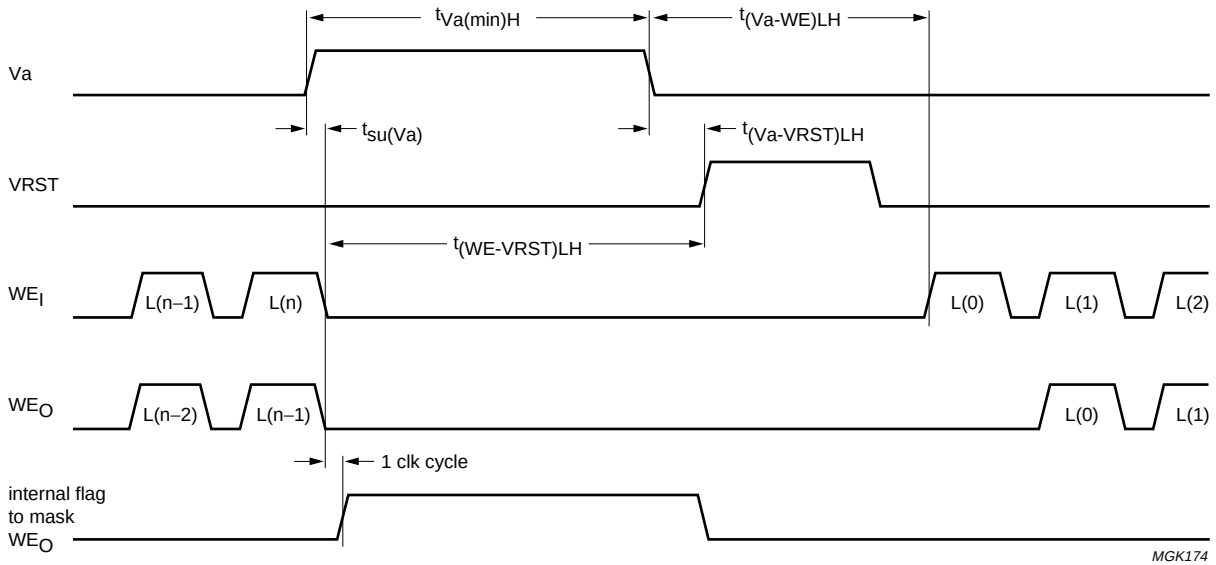


Fig.6 Timing diagram for WE_O blanking and Va.

Table 11 Va versus VRST

SYMBOL	PARAMETER	MIN.	UNIT
$t_{Va(min)H}$	minimum Va HIGH time	64	µs
$t_{su(Va)}$	set-up Va to negative edge of WE_I	0	µs
$t_{(Va-WE)LH}$	Va LOW to WE_I HIGH time	0	µs
$t_{(Va-VRST)LH}$	Va LOW to VRST HIGH time	0	µs
$t_{(WE-VRST)LH}$	WE_I LOW to VRST HIGH time	64	µs

LIST OF SNERT BUS ADDRESSES USED IN LIMERIC

TASTE register

Table 12 TASTE register usage

USE	ACTION
Purpose	to set 4 different types of noise reduction
Address	F3
Read/write	write
Range	0 to 4; **0** = noise filtering disabled

Table 13 TASTE register content

MSB							LSB	REMARK
0	0	0	0	ts3	ts2	ts1	ts0	see Table 14

Table 14 TASTE setting

TS3	TS2	TS1	TS0	FUNCTION
0	0	0	0	noise filtering disabled
0	0	0	1	not applicable
0	0	1	0	noise reduction; TASTE 1
0	0	1	1	not applicable
0	1	0	0	noise reduction; TASTE 2
0	1	0	1	not applicable
0	1	1	0	noise reduction; TASTE 3
0	1	1	1	not applicable
1	0	0	0	noise reduction; TASTE 4
1	0	0	1	not applicable
1	0	1	0	not applicable
1	0	1	1	not defined
1	1	0	0	not defined
1	1	0	1	not defined
1	1	1	0	not defined
1	1	1	1	not defined

Status register

Table 15 Status register usage

USE	ACTION
Purpose	internal settings
Address	F4
Read/write	write

Table 16 Status register content

MSB							LSB
Tctrl3	Tctrl2	Tctrl1	X	ExThr	Wv	DEM	WES

Table 17 Status register description

BIT	NAME	DESCRIPTION
0	WES	Write Enable Select 0: data coincides with write enable (both input and output) 1: data is delayed over one clock period with respect to the write enable (both input and output) see Fig.4
1	DEM	Demo Mode 0: demo mode disabled 1: demo mode on; the noise reduction circuit is switched on for the left half of the screen - the noise reduction is disabled (split screen function) for the right half of the screen
2	Wv	Weave 0: enable weave 1: disable weave
3	ExThr	External Threshold control bit 0: N_thr calculated by noise estimator 1: value of N_thr from register F9 is used
4	X	don’t care
5	Tctrl1	Test control 1 0: normal operation 1: test mode
6	Tctrl2	Test control 2 0: normal operation 1: test mode
5	Tctrl3	Test control 3 0: normal operation 1: test mode

W_{val} register (wanted value)

Table 18 W_{val} register usage

USE	ACTION
Purpose	register for setting up noise estimator
Address	F5
Read/write	write
Range	0 to 255

Table 19 W_{val} register

MSB							LSB	CONDITIONS
W_{val7}	W_{val6}	W_{val5}	W_{val4}	W_{val3}	W_{val2}	W_{val1}	W_{val0}	Tctrl2 = 0

Noise threshold register

Table 20 Noise threshold register usage

USE	ACTION
Purpose	register for setting the NTHR value for the noise filter externally
Address	F9
Read/write	write
Range	0 to 255

Table 21 Noise threshold register content

MSB							LSB
NTHR[7]	NTHR[6]	NTHR[5]	NTHR[4]	NTHR[3]	NTHR[2]	NTHR[1]	NTHR[0]

Noise estimator setting register

Table 22 Noise estimator setting register usage

USE	ACTION
Purpose	register for general setting of the noise estimator
Address	FA
Read/write	write

Table 23 Noise estimator setting register

MSB							LSB
YpScale1	YpScale0	0	0	0	0	0	0

Table 24 Noise estimator setting description

YpScale1	YpScale0	DESCRIPTION
0	0	noise estimator pre-filter gain setting = 1
0	1	noise estimator pre-filter gain setting = 0.5
1	0	noise estimator pre-filter gain setting = 0.25
1	1	noise estimator pre-filter bypassed

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD1}	supply voltage 1	–0.5	+6.5	V
V_{DD2}	supply voltage 2	–0.5	+6.5	V
V_I	input voltage	–0.5	+6.5	V
T_{stg}	storage temperature	–55	+150	°C
T_{amb}	operating ambient temperature	–40	+85	°C
P_{tot}	total power dissipation	–	150	mW
$P_{O(pin)}$	output power dissipation per output pin	–	100	mW

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	65	K/W

CHARACTERISTICS

V_{DD} = 5 V; T_{amb} = 25 °C; unless otherwise specified.

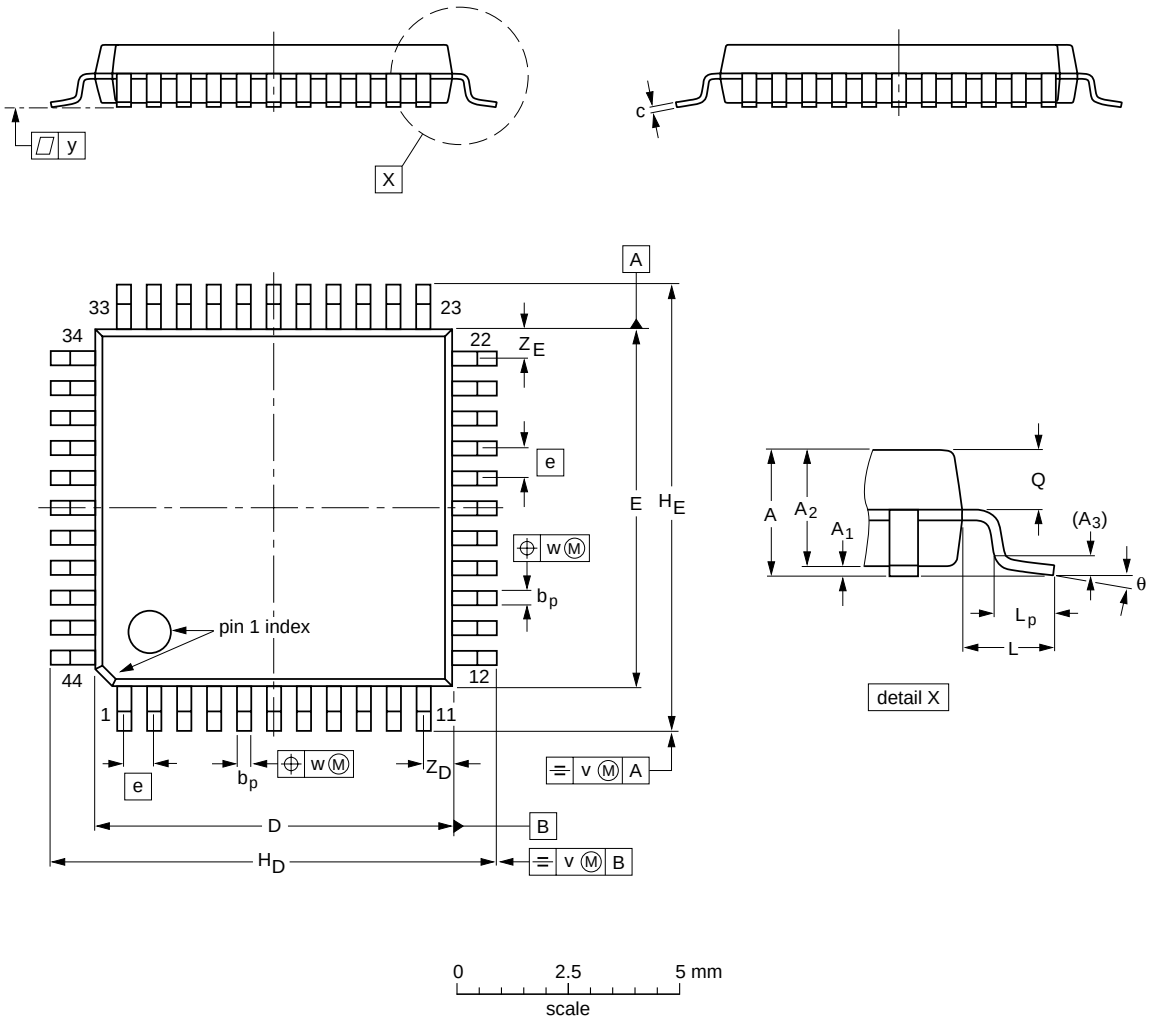
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage (pins 5, 29 and 30)		4.5	5.0	5.5	V
I_{DD}	supply current		–	70	–	mA
T_{amb}	operating ambient temperature		0	–	70	°C
T_{stg}	storage temperature		–50	–	+150	° C
P	power dissipation		–	350	–	mW
CLK						
f_{CLK}	clock frequency	±7%; note 1	10	16	17.1	MHz
δ	duty cycle		40	–	60	%
V_{IL}	LOW-level input voltage		–	–	0.8	V
V_{IH}	HIGH-level input voltage		2	–	–	V
C_L	load capacitance		10	–	–	pF
Y_{I7} to Y_{I0}, U_{I1}, U_{I2}, V_{I1}, V_{I0}, WE_I and Va						
V_{IL}	LOW-level input voltage		–	–	0.8	V
V_{IH}	HIGH-level input voltage		2.0	–	–	V
I_I	input current	V_I = 0 to 5 V	–	–	±20	μA
$t_{su(i)(D)}$	set-up time		6	–	–	ns
$t_{h(D)}$	hold time		7	–	–	ns
Y_{O7} to Y_{O0}, U_{O1}, U_{O2}, V_{O1}, V_{O0} and WE_O						
V_{OL}	LOW-level output voltage	I_{OL} = 1.6 mA	–	–	0.4	V
V_{OH}	HIGH-level output voltage	I_{OH} = 0.4 mA	2.4	–	–	V
$t_{h(Q)}$	output hold	C_L = 15 pF	7	–	–	ns
$t_{d(D)}$	output delay	C_L = 15 pF	–	–	32	ns
SNDA and SNCL						
f_{SNERT}	bus clock frequency		–	–	1	MHz
V_{IL}	LOW-level input voltage		–	–	0.8	V
V_{IH}	HIGH-level input voltage		2.0	–	–	V
V_{OL}	LOW-level output voltage		–	–	0.4	V
V_{OH}	HIGH-level output voltage		2.4	–	–	V
TST0, TST1 and TST2						
V_{IL}	LOW-level input voltage		–	–	0.8	V
V_{IH}	HIGH-level input voltage		2.0	–	–	V

Note

1. Maximum number of clocks per line is 1024.

PACKAGE OUTLINE

QFP44: plastic quad flat package; 44 leads (lead length 1.3 mm); body 10 x 10 x 1.75 mm **SOT307-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	Q	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	2.10	0.25 0.05	1.85 1.65	0.25	0.40 0.20	0.25 0.14	10.1 9.9	10.1 9.9	0.8	12.9 12.3	12.9 12.3	1.3	0.95 0.55	0.85 0.75	0.15	0.15	0.1	1.2 0.8	1.2 0.8	10^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT307-2						~~92-11-17~~ 95-02-04

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

Reflow soldering

Reflow soldering techniques are suitable for all QFP packages.

The choice of heating method may be influenced by larger plastic QFP packages (44 leads, or more). If infrared or vapour phase heating is used and the large packages are not absolutely dry (less than 0.1% moisture content by weight), vaporization of the small amount of moisture in them can cause cracking of the plastic body. For more information, refer to the Drypack chapter in our *"Quality Reference Handbook"* (order code 9398 510 63011).

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

Wave soldering

Wave soldering is **not** recommended for QFP packages. This is because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

If wave soldering cannot be avoided, the following conditions must be observed:

- **A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.**
- **The footprint must be at an angle of 45° to the board direction and must incorporate solder thieves downstream and at the side corners.**

Even with these conditions, do not consider wave soldering the following packages: QFP52 (SOT379-1), QFP100 (SOT317-1), QFP100 (SOT317-2), QFP100 (SOT382-1) or QFP160 (SOT322-1).

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

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